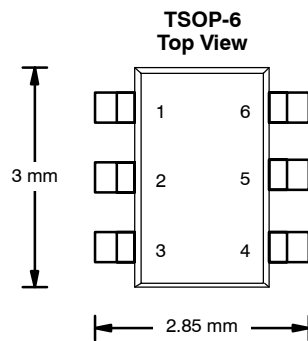


## N-Channel 100-V (D-S) MOSFET

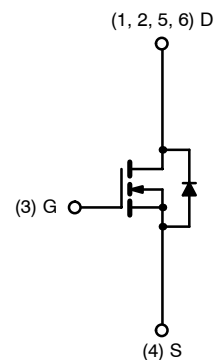
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.170 @ $V_{GS} = 10$ V	2.4
	0.185 @ $V_{GS} = 6.0$ V	2.3

### FEATURES

- High-Efficiency PWM Optimized
- 100%  $R_g$  Tested



Ordering Information: Si3430DV-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	100		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	2.4	1.8	A
		$T_A = 85^\circ\text{C}$	1.7	1.3	
Pulsed Drain Current	$I_{DM}$	8			
Avalanche Current	$I_{AR}$	6			
Repetitive Avalanche Energy (Duty Cycle $\leq 1\%$ )	$E_{AR}$	L = 0.1 mH	1.8		mJ
Continuous Source Current (Diode Conduction) <sup>a</sup>			$I_S$	1.7	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.0	1.14	W
		$T_A = 85^\circ\text{C}$	1.0	0.59	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 5$ sec	45	62.5	$^\circ\text{C/W}$
		Steady State	90	110	
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	25	30		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

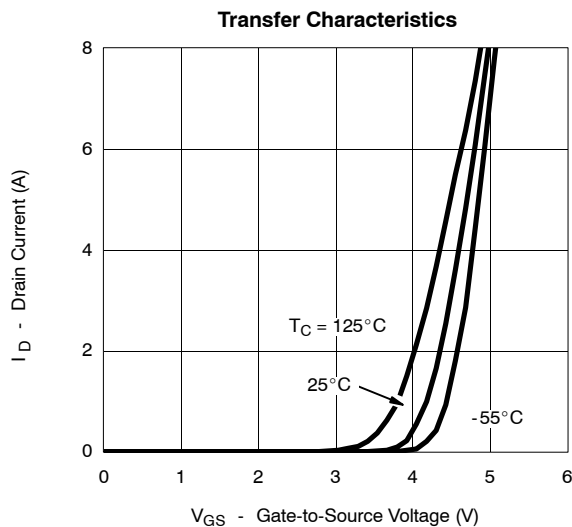
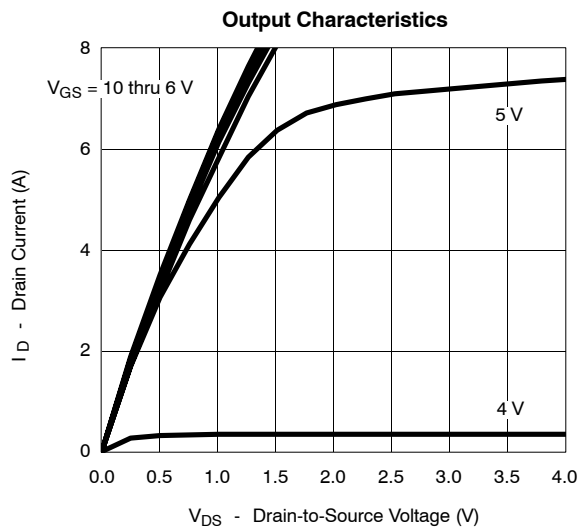
**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			25	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	8			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.4 A		0.148	0.170	Ω
		V <sub>GS</sub> = 6.0 V, I <sub>D</sub> = 2.3 A		0.160	0.185	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.4 A		7		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.4 A		5.5	6.6	nC
Gate-Source Charge	Q <sub>gs</sub>			1.5		
Gate-Drain Charge	Q <sub>gd</sub>			1.4		
Gate Resistance	R <sub>g</sub>		1		4	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 50 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		9	20	ns
Rise Time	t <sub>r</sub>			11	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			16	30	
Fall Time	t <sub>f</sub>			9	20	
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 0.1 V, f = 5 MHz		2.8		Ω
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.7 A, di/dt = 100 A/μs		50	80	ns

Notes

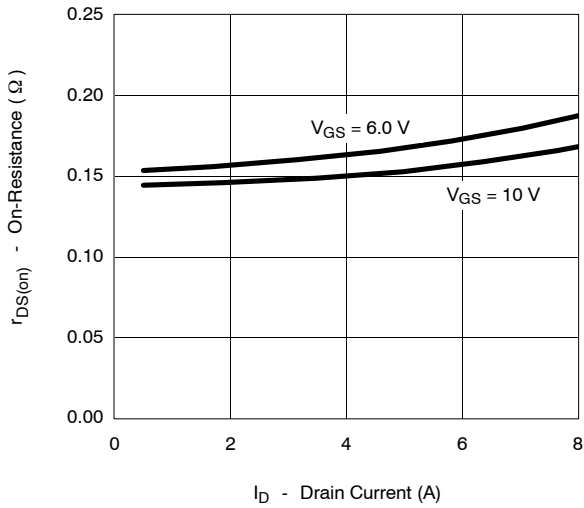
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

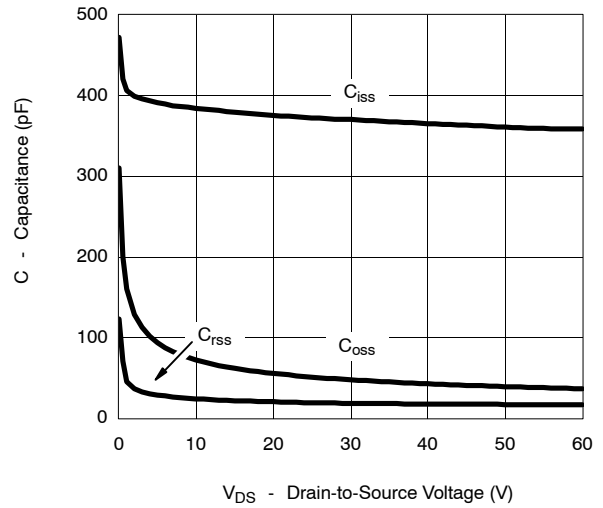


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

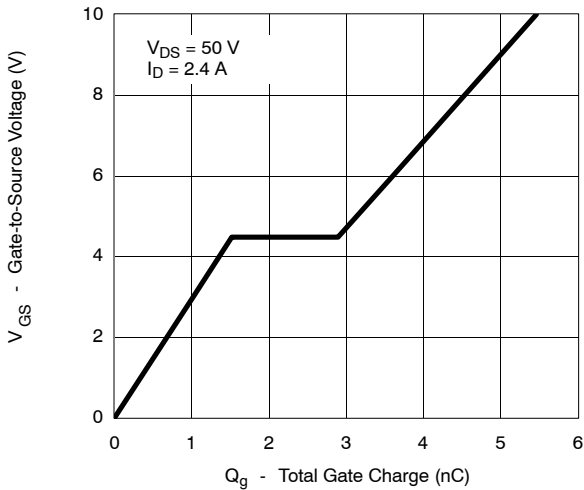
**On-Resistance vs. Drain Current**



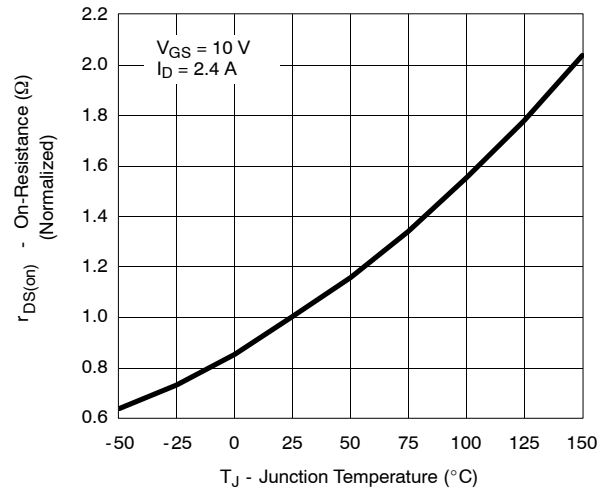
**Capacitance**



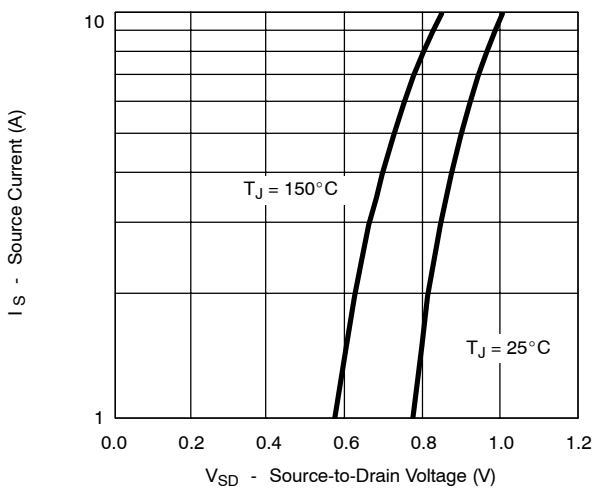
**Gate Charge**



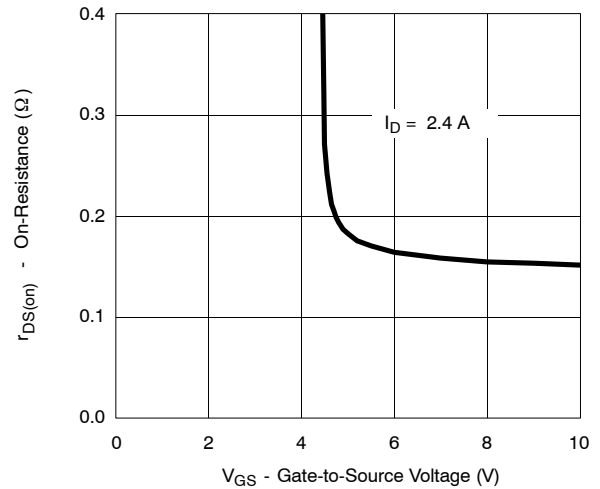
**On-Resistance vs. Junction Temperature**



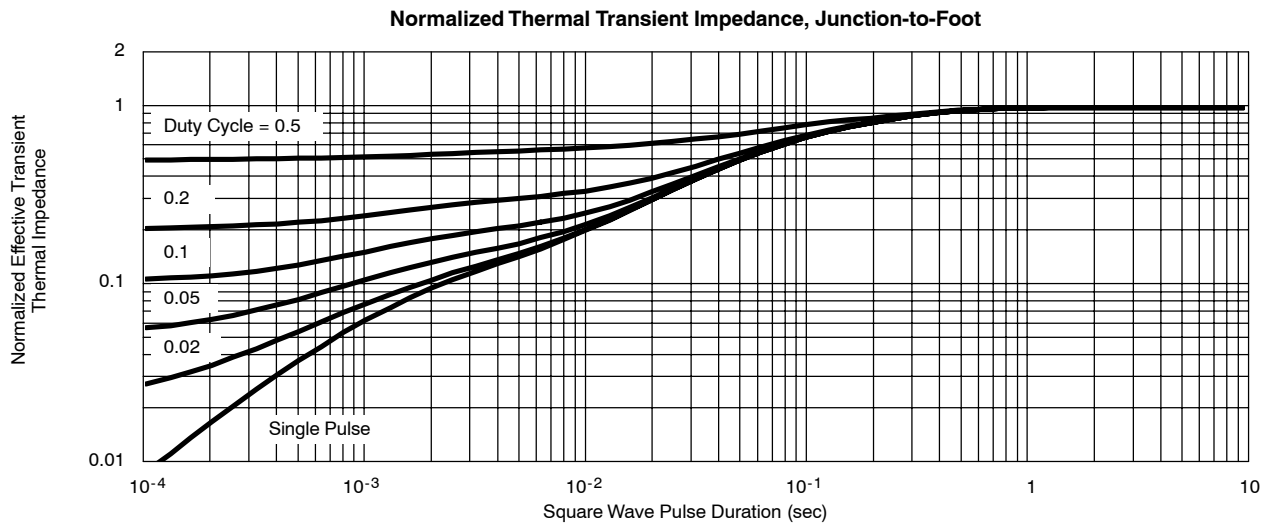
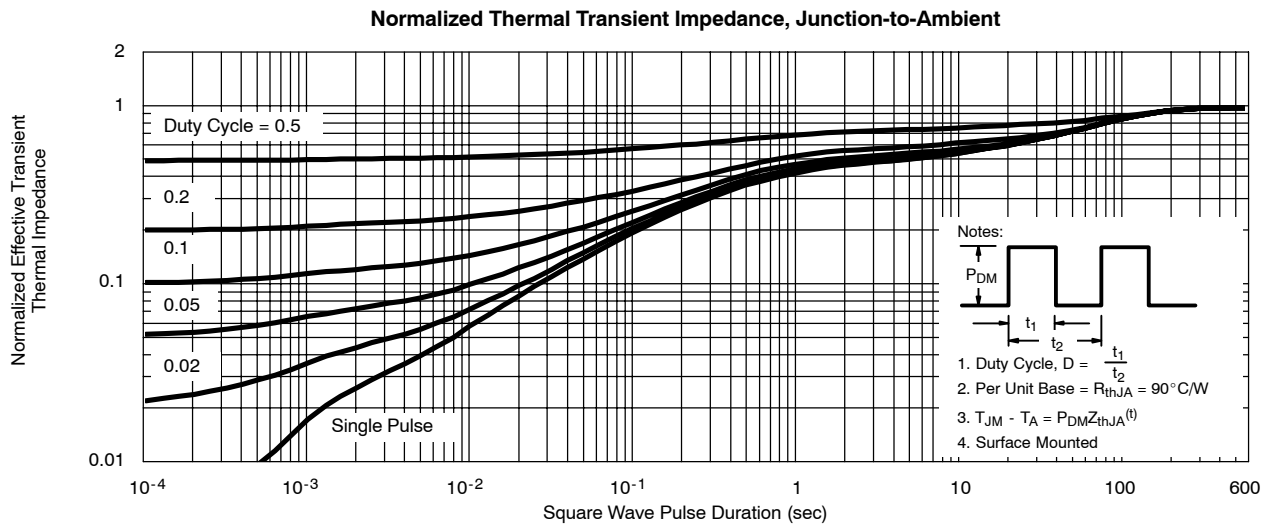
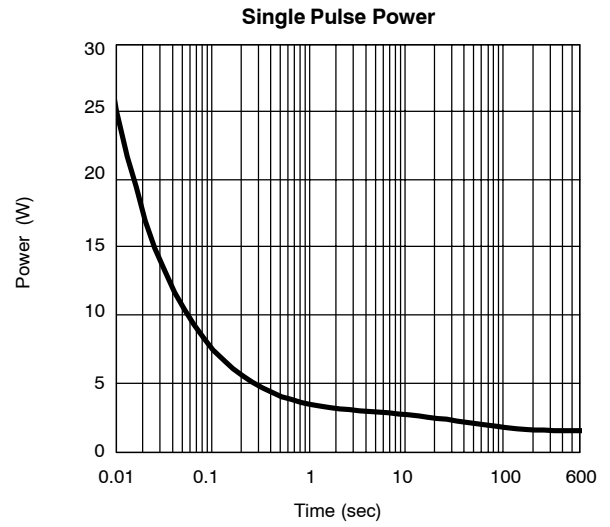
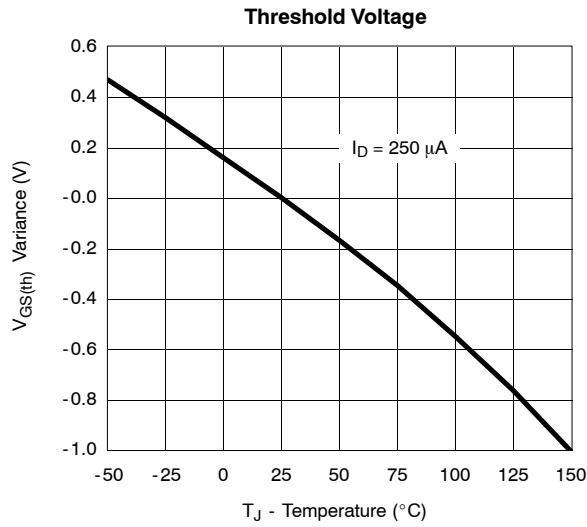
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**





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